What is Claimed:

1. A delay-locked loop (DLL) comprising:

a variable delay line arrangement operable to receive a reference clock and to output a delayed local clock;

a phase comparator device operable to compare said reference clock and said local clock and to provide an up/down indication; and

a delay control circuit, responsive to said up/down count-indication, to provide a reduced-noise delay control signal to said variable delay line arrangement, said delay control circuit being operable to count said up/down indication using an escalator code arrangement.

2. The DLL of claim 1, wherein said delay control circuit includes:

an escalator code generator, responsive to an externally-provided count trigger signal, to generate an escalator code; and

an escalator-code-to-analog converter (ECAC) to convert said escalator code from said generator.

3. The DLL of claim 2, wherein said generator is arranged to

represent base 10 numbers with a mixed code having a coin code portion and a cash code portion so as to eliminate multi-bit changes in the cash code portion upon changes in count direction, said coin code corresponding to one or more of the least significant bits of said cash code but fewer than all bits of said cash code; and

represent a count in a first direction as a summation of the base 10 number represented by said coin code and the base 10 number represented by said cash code;

4. The DLL of claim 3, wherein said coin code is a thermometer code. and said cash code is a binary-weighted code.

5. The DLL of claim 3, wherein said cash code is one of a binary-weighted code and a thermometer code.

6. A delay-locked loop (DLL) comprising:

variable delay line means for receiving a reference clock and outputting a delayed a local clock;

phase comparator means for comparing said reference clock and said local clock and to provide an up/down indication; and

delay control means, responsive to said up/down count-indication, for providing a reduced-noise delay control signal to said variable delay line arrangement, said delay control circuit being operable to count said up/down indication using an escalator code arrangement.

7. A memory device including the DLL of claim 1.

8. The memory device of claim 7, wherein said memory device is a synchronous DRAM.